THAT WHICH IS CLAIMED IS:

1. An integrated circuit device, comprising:

a CAM array block that is configured to perform a search operation in a staged segment-to-segment manner using a plurality of hybrid comparands that are pipelined into said CAM array block during consecutive stages of the search operation, with each of the plurality of hybrid comparands comprising a virtual sector field and a data field.

2. The device of Claim 1, wherein said CAM array block is responsive to a segment address, which identifies an active segment of CAM cells in said CAM array block.

3. The device of Claim 1, wherein said CAM array block comprises:

a CAM array; and

a global mask cell sub-array that is electrically coupled to said CAM array.

4. The device of Claim 3, wherein said CAM array block further comprises:

a bit/data line control circuit that is electrically coupled to said CAM array by bit lines and data lines and has inputs that are responsive mask assertion signals generated by said global mask cell sub-array.

5. The device of Claim 2, wherein the data field is derived from a first portion of an input address; and wherein the virtual sector field and the segment address are derived from a second portion of the input address.

6. An integrated circuit device, comprising:

a CAM array block that is configured to perform a search operation in a staged segment-to-segment manner using a plurality of comparands that are pipelined into said CAM array block during consecutive stages of the search operation, said CAM array block comprising at least one multi-segment CAM array and a global mask cell sub-array that is responsive to a segment address.

7. The device of Claim 6, wherein said global mask cell sub-array is responsive to a mode select signal.

8. The device of Claim 6, wherein the comparands are hybrid comparands that comprise a virtual sector field and a data field.

9. An integrated circuit system, comprising:

a programmable address translation unit that is configured to generate a CAM segment address and a virtual sector address in response to a first portion of an input address; and

a CAM device that is responsive to the CAM segment address and is configured to treat the virtual sector address and a second portion of the input address as respective fields of a search word during pipelined search operations.

10. The system of Claim 9, wherein said CAM device comprises a CAM array block having a global mask cell sub-array therein that is responsive to the CAM segment address.

11. A content address memory (CAM) device, comprising:

a CAM array having a plurality of segments therein;

a bit/data line control circuit that is electrically coupled to said CAM array by bit lines and data lines; and

a global mask cell sub-array that is electrically coupled to said bit/data line control circuit and is responsive to a segment address signal that designates which ones of the plurality of segments are active and which other ones of the plurality of segments are globally masked during a staged segment-to-segment search operation.

12. The CAM device of Claim 11, wherein said global mask cell sub-array is further responsive to a mode select signal that specifies an active width of search words applied to said CAM array during search operations.

13. The CAM device of Claim 11, wherein said global mask cell sub-array is electrically coupled to the bit lines.

14. An integrated circuit system, comprising:

a programmable address translation unit that is configured to generate a CAM segment address in response to a first portion of an input address; and

a CAM device that is responsive to a second portion of the input address, said CAM device comprising:

a segmented CAM array; and

a global mask cell sub-array that is configured to specify location of global masks provided to said segmented CAM array during search operations and is responsive to the CAM segment address.

15. The system of Claim 14, wherein the CAM segment address designates which portions of said segmented CAM array are actively searched and which other portions of said segmented CAM array are globally masked during a respective search operation.

16. The system of Claim 14, wherein said CAM device further comprises a bit/data line control circuit that is electrically coupled to said segmented CAM array by bit lines and data lines.

17. The system of Claim 16, wherein said bit/data line control circuit is configured to receive mask assertion signals from said global mask cell sub-array.

18. The system of Claim 14, wherein said global mask cell sub-array is responsive to a mode select signal.

19. The system of Claim 14, wherein said segmented CAM array comprises XY ternary CAM cells.

20. The system of Claim 14, wherein said global mask cell sub-array comprises hard and soft mask cells therein.

21. The system of Claim 14, wherein said programmable address translation unit is further configured to generate a virtual sector address in response to the first portion of the input address; and wherein said CAM device is configured to treat the second portion of the input address and the virtual sector address as a hybrid comparand during a search operation.

22. A method of operating a CAM array, comprising the step of:

performing a search operation in a staged segment-to-segment manner across a CAM array using a plurality of hybrid comparands that are pipelined into the CAM array during consecutive stages of the search operation, with each of the plurality of hybrid comparands comprising a virtual sector field and a data field.

23. The method of Claim 22, wherein said performing step comprises:

applying a virtual sector field of a first hybrid comparand to a first plurality of data lines that are electrically coupled to a first segment of CAM cells in the CAM array, while concurrently applying a data field of a second hybrid comparand to a second plurality of data lines that are electrically coupled to a second segment of CAM cells in the CAM array.

24. The method of Claim 23, wherein said applying step comprises applying the virtual sector field of the first hybrid comparand to the first plurality of data lines while concurrently globally masking a third plurality of data lines that are electrically coupled to a third segment of CAM cells in the CAM array.

25. The method of Claim 22, wherein said performing step comprises:

applying a virtual sector field and a first data field of a first hybrid comparand to a first plurality of data lines that are electrically coupled to a first segment of CAM cells in the CAM array, while concurrently applying a second data field of a second hybrid comparand to a second plurality of data lines that are electrically coupled to a second segment of CAM cells in the CAM array.

26. The method of Claim 25, wherein said applying step comprises applying the virtual sector field and the first data field of the first hybrid comparand to the first plurality of data lines while concurrently globally masking a third plurality of data lines that are electrically coupled to a third segment of CAM cells in the CAM array.

27. A method of operating an integrated circuit system, comprising the steps of:

decoding a first portion of a first input address into sector, sub-sector and virtual sector addresses; and

performing a search operation in a sector of a CAM device that is designated by the sector address, by applying a first hybrid comparand comprising the virtual sector address and a second portion of the first input address, to first data lines that are electrically coupled to a CAM array within the sector.

28. The method of Claim 27, wherein said performing step comprises performing a pipelined search operation in the sector by applying the first search word while concurrently applying a portion of a second hybrid comparand to second data lines that are electrically coupled to the CAM array.

29. An integrated circuit system, comprising:

a multi-port memory array containing packet header data therein;

funnel logic that is configured to generate a N-bit comparand comprising portions of at least two header fields read from distinct locations in said multi-port memory array;

a content addressable memory device that is configured to generate an index in response to application of the N-bit comparand during a search operation; and

a memory device comprising an entry of microcode therein that is partitioned into at least a first field that identifies a write address in said multi-port memory array to which the index or data derived from using the index as a pointer is to be written.

30. The system of Claim 29, wherein said funnel logic comprises:

a multiplexer that is configured to receive read data from said multi-port memory array; and

a map table that is configured to pass select signals to said multiplexer, in response to a read address derived from a bit map field within the entry of microcode.

31. A content addressable memory (CAM) array, comprising:

a row of CAM cells having at least xR and xS segments of CAM cells therein that include xR and xS match line segments, respectively, where 2R and 2S are positive integers; and

a dual-capture match line signal repeater that is configured to isolate the xR and xS match line segments from each other during a first evaluation time interval, pass a match signal from the xR match line segment to the xS match line segment during a first capture time interval and pass a late miss signal from the xR match line segment to the xS match line segment during a second capture time interval that terminates after termination of the first capture time interval.

32. The CAM array of Claim 31, wherein the second capture time interval commences upon termination of the first capture time interval; and wherein said dual-capture match line signal repeater is further configured to block transfer of the match signal from the xR match line segment to the xS match line segment during the second capture time interval.

33. The CAM array of Claim 31, wherein the first and second capture time intervals overlap in time; and wherein said dual-capture match line signal repeater is further configured to block transfer of the match signal from the xR match line segment to the xS match line segment during at least a portion of the second capture time interval.

34. The CAM array of Claim 31, wherein said dual-capture match line signal repeater comprises:

a first inverter having an input electrically connected to the xR match line segment; and

a second inverter having an input electrically coupled to an output of said first inverter and a tri-state output electrically coupled to the xS match line segment, said second inverter responsive to a first evaluation control signal and a first connect control signal.

35. The CAM array of Claim 34, wherein the first evaluation control signal is an active low signal and the first connect control signal is an active high signal.

36. The CAM array of Claim 35, wherein a falling edge of the first evaluation control signal signifies commencement of the first capture time interval; and wherein a rising edge of the first connect control signal signifies commencement of the second capture time interval.

37. The CAM array of Claim 31, further comprising:

a pair of PMOS pull-up transistors electrically connected in series between the xR match line segment and a power supply line, said pair of PMOS pull-up transistors comprising a first PMOS pull-up transistor having a gate terminal that is responsive to a PBIAS signal and a second PMOS pull-up transistor having a gate terminal that is electrically connected to an output of said first inverter.

38. The CAM array of Claim 31, further comprising:

a PMOS precharge transistor having a first current carrying terminal electrically connected to the xR match line segment, a second current carrying terminal electrically coupled to a power supply line and a gate terminal that is responsive to a zeroth evaluation control signal.

39. The CAM array of Claim 38, wherein said dual-capture match line signal repeater comprises:

a first inverter having an input electrically connected to the xR match line segment; and

a second inverter having an input electrically coupled to an output of said first inverter and a tri-state output electrically coupled to the xS match line segment, said second inverter responsive to a first evaluation control signal and a first connect control signal.

40. The CAM array of Claim 31, wherein the first evaluation time interval is synchronized to a zeroth evaluation control signal, the first capture time interval is synchronized to a first evaluation control signal and the second capture time interval is synchronized to a first connect control signal.

41. A content addressable memory (CAM) array, comprising:

a row of CAM cells having at least xR, xS and xT segments of CAM cells therein that include xR, xS and xT match line segments, respectively, where 2R, 2S and 2T are positive integers;

a first dual-capture match line signal repeater that is configured to isolate the xR and xS match line segments from each other during an first evaluation time interval, pass a match signal from the xR match line segment to the xS match line segment during a first early capture time interval and pass a late miss signal from the xR match line segment to the xS match line segment during a first late capture time interval that terminates after termination of the first early capture time interval; and

a second dual-capture match line signal repeater that is configured to isolate the xS and xT match line segments from each other during a second evaluation time interval, pass a match signal from the xS match line segment to the xT match line segment during a zeroth early capture time interval and pass a late miss signal from the xS match line segment to the xT match line segment during a zeroth late capture time interval that terminates after termination of the zeroth early capture time interval.

42. The CAM array of Claim 41, wherein the first late capture time interval and the first early capture time interval do not overlap in time.

43. The CAM array of Claim 41, wherein said first dual-capture match line signal repeater comprises:

a first inverter having an input electrically connected to the xR match line segment; and

a second inverter having an input electrically coupled to an output of said first inverter and a tri-state output electrically coupled to the xS match line segment, said second inverter responsive to a first evaluation control signal and a first connect control signal.

44. The CAM array of Claim 43, wherein said second dual-capture match line signal repeater comprises:

a third inverter having an input electrically connected to the xS match line segment; and

a fourth inverter having an input electrically coupled to an output of said third inverter and a tri-state output electrically coupled to the xT match line segment, said fourth inverter responsive to a zeroth evaluation control signal and a zeroth connect control signal.

45. The CAM array of Claim 44, further comprising:

a PMOS precharge transistor having a first current carrying terminal electrically connected to the xR match line segment, a second current carrying terminal electrically coupled to a power supply line and a gate terminal that is responsive to the zeroth evaluation control signal.

46. A method of searching a CAM array, comprising the steps of:

precharging a first match line segment that is connected to a first segment of CAM cells in a first row of the CAM array; and

performing a staged search operation by:

applying a first segment of a search word to first data lines that are electrically coupled to the first segment of CAM cells while concurrently isolating the first match line segment from a second match line segment that is connected to a second segment of CAM cells in the first row of the CAM array;

passing a match signal from the first match line segment to the second match line segment, during a first capture time interval; and

correcting an erroneous capture of the match signal by passing a late miss signal from the first match line segment to the second match line segment during a second capture time interval that terminates after termination of the first capture time interval.

47. The method of Claim 46, wherein said step of passing a late miss signal is performed concurrently with a step of applying a second segment of the search word to second data lines that are electrically coupled to the second segment of CAM cells.

48. The method of Claim 47, wherein said step of passing a match signal is performed concurrently with a step of globally masking the second data lines.

49. The method of Claim 48, wherein said step of passing a match signal is performed in-sync with a first evaluation control signal; and wherein said step of correcting an erroneous capture is performed in-sync with a first connect control signal.

50. The method of Claim 46, wherein said step of passing a match signal is performed in-sync with a first evaluation control signal; and wherein said step of correcting an erroneous capture is performed in-sync with a first connect control signal.

51. A method of searching a CAM array having first, second, third and fourth segments of CAM cells therein, comprising the steps of:

applying a first segment of a search word to first data lines that are electrically coupled to the first segment of CAM cells while simultaneously applying a third segment of a prior search word to third data lines that are electrically coupled to the third segment of CAM cells;

passing an first match signal from a first match line segment associated with the first segment of CAM cells to a second match line segment associated with the second segment of CAM cells, while concurrently passing a second match signal from a third match line segment associated with the third segment of CAM cells to a fourth match line segment associated with the fourth segment of CAM cells, during a first capture time interval; and

passing a first late miss signal from the first match line segment to the second match line segment and a second late miss signal from the third match line segment to the fourth match line segment, during a second capture time interval that terminates after termination of the first capture time interval.

52. The method of Claim 51, wherein the first and second capture time intervals are nonoverlapping.

53. A content addressable memory (CAM) array, comprising:

a row of CAM cells comprising first and second match line segments; and

a dual-capture match line signal repeater electrically connected to the first and second match line segments, said repeater comprising:

a first inverter having an input electrically coupled to the first match line segment; and

a second inverter having an input electrically coupled to an output of said first inverter and a tri-state output electrically coupled to the second match line segment.

54. The CAM array of Claim 53, wherein said second inverter is responsive to an evaluation control signal and a connect control signal.

55. The CAM array of Claim 54, wherein a pull-up path in said second inverter is enabled when the evaluation control signal is active; and wherein a pull-down path in said second inverter is enabled when the connect control signal is active.

56. The CAM array of Claim 55, wherein the evaluation control signal is an active low signal; and wherein the connect control signal is an active high signal.

57. A content addressable memory (CAM) array, comprising:

a row of CAM cells having at least xR and xS segments of CAM cells therein that include xR and xS match line segments, respectively, where 2R and 2S are positive integers; and

a dual-capture match line signal repeater that is configured to:

transfer a match signal from the xR match line segment to the xS match line segment during an early capture time interval while simultaneously blocking transfer of a miss signal from the xR match line segment to the xS match line segment; and

transfer the miss signal from the xR match line segment to the xS match line segment during a late capture time interval that terminates after termination of the early capture time interval.

58. The CAM array of Claim 57, wherein said dual-capture match line signal repeater is further configured to block transfer of the match signal from the xR match line segment to the xS match line segment during at least a portion of the late capture time interval.

59. The CAM array of Claim 58, wherein the late capture time interval commences upon termination of the early capture time interval.

60. The CAM array of Claim 57, wherein said dual-capture match line signal repeater is further configured to block transfer of the match signal from the xR match line segment to the xS match line segment during the entire late capture time interval.

61. The CAM array of Claim 58, wherein said dual-capture match line signal repeater comprises an inverter having a tri-state output that is electrically connected to the xS match line segment.

62. A method of performing a pipelined search operation within a segmented CAM array, comprising the steps of:

applying a first segment of a search word to first data lines that are electrically coupled to the first segment of CAM cells during a first stage of the pipelined search operation; then

passing a match signal from a first match line segment associated with the first segment of CAM cells to a second match line segment associated with a second segment of CAM cells, while second data lines that are electrically coupled to the second segment of CAM cells are being globally masked; and then

applying a second segment of the search word to the second data lines during a second stage of the pipelined search operation, while simultaneously passing a late miss signal from the first match line segment to the second match line segment to thereby discharge the second match line segment.

63. A method of performing a pipelined search operation within a segmented CAM array, comprising the steps of:

passing an early match signal from a first segment of CAM cells to a second segment of CAM cells during a first stage of a pipelined search operation; and

passing a late miss signal from the first segment of CAM cells to the second segment of CAM cells during a second stage of the pipelined search operation.

64. The method of Claim 63, wherein said step of passing a late miss signal comprises passing a late miss signal in-sync with applying a second segment of a search word to data lines coupled to the second segment of CAM cells.

65. The method of Claim 64, wherein said step of passing an early match signal comprises passing an early match signal in-sync with globally masking data lines coupled to the second segment of CAM cells.

66. The method of Claim 63, wherein said step of passing an early match signal comprises passing an early match signal in-sync with globally masking data lines coupled to the second segment of CAM cells.

67. A content addressable memory (CAM) device, comprising:

at least two sectors of CAM array blocks that are sector addressable during search operations according to the parity of a search word applied to the CAM device.

68. The CAM device of Claim 67, wherein said at least two sectors of CAM array blocks comprise at least four sectors that are sector addressable during search operations according to the parity of the search word.

69. The CAM device of Claim 67, further comprising a sector address generator that is configured to generate a parity-based sector address in response to an input value comprising at least some portion of a search word.